CLAIMS

What is claimed is:

1. An apparatus to generate a bit clock synchronized with a digital signal, comprising:

an edge detecting unit detecting edges of the digital signal;

a first edge counter counting a number of the detected edges during a first period;

a second edge counter counting the number of the detected edges during a second period;

a first counter counting the number of the edges of a system clock if one of the edges is detected during the first period; and

a bit clock generating unit generating the bit clock based on the counted number of the first counter or at a channel bit interval, if the counted number of one of the first edge counter and second edge counter is equal to a first predetermined value.

2. The apparatus of claim 1, wherein the first edge counter disregards the edges detected during a period other than the first period, and the second edge counter disregards the edges detected during the period other than the second period.

3. The apparatus of claim 1, wherein the bit clock generating unit gives priority to the count value of the first counter over the channel bit interval.

4. The apparatus of claim 2, wherein the bit clock generating unit generates the bit clock irrespective of the channel bit interval if the first counter is reset.

5. The apparatus of claim 1, wherein the first period is set based on the count value of the first counter.

6. The apparatus of claim 5, wherein, if the edge detecting unit detects a first edge of the digital signal, the first counter is reset and counts the system clock, where the first counter is reset every time the first edge is detected during the first period.

7. The apparatus of claim 6, further comprising:

a first window signal generating unit generating a first window signal as a signal indicating the first period based on the count value of the first counter and outputting the first window signal to the first edge counter.

8. The apparatus of claim 7, further comprising:

a second counter wherein, if one of the edges is detected during a period other than the first window signal period after the first edge is detected, the second counter is reset, counts the system clock, and is reset every time the one of the edges is detected during the second period.

9. The apparatus of claim 8, wherein the second period is set based on the count value of the second counter.

10. The apparatus of claim 8, further comprising:

a second window signal generating unit generating a second window signal as a signal indicating the second period based on the count value of the second counter and outputting the second window signal to the second edge counter.

11. The apparatus of claim 8, further comprising:

a state managing unit monitoring outputs of the first counter, the second counter, the edge detecting unit, the first edge counter, and the second edge counter and managing a state of the apparatus generating the bit block.

12. The apparatus of claim 11, wherein the state is one of a bit clock unlock state, a bit clock lock ready state, and a bit clock lock state.

13. The apparatus of claim 12, wherein the state managing unit sets the state of the apparatus generating the bit clock as the bit clock unlock state if the edges of the digital signal is detected by the edge detecting unit, one of the count values of the first counter and second counter is equal to a second predetermined value in the bit clock lock ready state, or the count value of the first counter is equal to a third predetermined value in the bit clock lock state.

14. The apparatus of claim 12, wherein the state managing unit sets the state of the apparatus generating the bit clock as the bit clock lock ready state if the first edge is detected by the edge detecting unit in the bit clock unlock state, and sets the state of the apparatus generating the bit clock as the bit clock lock state if one of the count values of the first counter and second counter is equal to the first predetermined value in the bit clock lock ready state.

15. The apparatus of claim 14, wherein, in the bit clock lock ready state, the bit clock generating unit generates the bit clock based on one of the count value of the first counter and the channel bit interval.

16. The apparatus of claim 12, wherein, in the bit clock unlock state, the bit clock generating unit generates the bit clock by the channel bit interval.

17. The apparatus of claim 1, further comprising:

a state managing unit setting a state of the apparatus generating the bit clock as the bit clock lock state if one of the counts of the first edge counter and the second edge counter is equal to the first predetermined value.

18. An apparatus generating a bit clock synchronized with digital data reproduced from a disc in a disk drive, comprising:

an edge detecting unit detecting edges of the digital data;

a first edge counter counting a number of the edges detected during a first period after the first edge is detected by the edge detecting unit;

a second edge counter counting the number of the edges detected during a second period, after the first edge is detected and the edge are detected during a period other than the first period;

a first counter counting a system clock if the edge is detected during the first period; and

a bit clock generating unit generating the bit clock based on one of count values of the first counter and a channel bit interval, if the count value of the first counter and second counter is equal to a first predetermined value, and a state of the apparatus is set as the bit clock lock state.

19. The apparatus of claim 18, wherein the bit clock generating unit gives priority to the count value of the first counter over the channel bit interval.

20. A disk driver having a disk, comprising:

a pick-up unit picking up data from the disk and outputting a high frequency signal;

a radio frequency (RF) amplifying unit amplifying the high frequency signal to a predetermined level;

a digital signal processor (DSP) receiving the amplified signal to the amplified high frequency signal into a digital signal;

a digital filter filtering the noise from the digital signal;

a decoder decoding the filtered digital signal in synchronization for an input bit clock with error correction on the filtered digital signal; and

a bit clock generation apparatus comprising

an edge detecting unit detecting edges of the digital signal,

a first edge counter counting a number of the detected edges during a first period,

a second edge counter counting the number of the detected edges during a second period,

a first counter counting a system clock if the edges are detected during the first period, and

a bit clock generating unit generating the bit clock based on a count value of the first counter or at a channel bit interval, if one of the counts of the first edge counter and second edge counter is equal to a first predetermined value.

21. The disk driver of claim 20, wherein the first edge counter disregards the edges detected during a period other than the first period, and the second edge counter disregards the edges detected during the period other than the second period.

22. The disk driver of claim 20, wherein the bit clock generating unit gives priority to the count value of the first counter over the channel bit interval.

23. The disk driver of claim 21, wherein the bit clock generating unit generates the bit clock irrespective of the channel bit interval if the first counter is reset.

24. The disk driver of claim 20, wherein the first period is set based on the count value of the first counter.

25. The disk driver of claim 24, wherein, if the edge detecting unit detects a first edge of the digital signal, the first counter is reset and counts the system clock, where the first counter is reset every time the first edge is detected during the first period.

26. The disk driver of claim 25, further comprising:

a first window signal generating unit generating a first window signal as a signal indicating the first period based on the count value of the first counter and outputting the first window signal to the first edge counter.

27. The disk driver of claim 26, further comprising:

a second counter, wherein, if one of the edges is detected during a period other than the first window signal period after the first edge is detected, the second counter is reset, counts the system clock, and is reset every time the one of the edges is detected during the second period.

28. The disk driver of claim 27, further comprising:

a second window signal generating unit generating a second window signal as a signal indicating the second period based on the count value of the second counter and outputting the second window signal to the second edge counter.

29. The disk driver of claim 27, further comprising:

a state managing unit monitoring outputs of the first counter, the second counter, the edge detecting unit, the first edge counter, and the second edge counter and managing a state of the apparatus generating the bit block.

30. A method of generating a bit clock in a digital data generating system, the method comprising:

detecting edges of a digital signal;

generating a first edge count value by counting a number of the edges detected during a first period;

generating a second edge count value by counting the number of the edges detected during a second period;

setting a state of the digital data generating system as a bit clock lock state if one of the first edge count value and second edge count value is equal to a first predetermined value; and

generating the bit clock using one of the channel bit interval and a first count value, wherein the first count value is reset and generated by counting a system clock every time the edges are detected during the first period in the bit clock lock state.

31. The method of claim 30, wherein the first period is set by using a first window signal generated based on a first count value created when a first edge is detected.

32. The method of claim 31, wherein the second period is set by using a second window signal generated based on a second count value, where the second count value is reset and created by counting the system clock when the first edge is detected during a period other than the first period, and the second count value is reset every time one of the edges is detected during the second period.

33. The method of claim 30, further comprising:

disregarding the edges detected during periods other than the first period and second period.

34. The method of claim 30, wherein generating the bit clock is performed while giving priority to the first count value.

35. A method of generating a bit clock synchronized with a digital signal generated in a digital data generating system, the method comprising:

generating the bit clock by a channel bit interval in a bit clock unlock state;

converting the bit clock unlock state into a bit clock lock ready state if a first edge of the digital signal is detected;

generating a first edge count value by counting a number of edges detected during a first period in the bit clock lock ready state;

generating a second edge count value by counting the number of the edges detected during a second period in the bit clock lock ready state;

converting the bit clock lock ready state into a bit clock lock state if the first edge count value or the second edge count value is equal to a first predetermined value; and

generating the bit clock based on one of a first count value, wherein the first count value is reset and generated by counting a system clock every time one of the edges is detected during the first period in the bit clock lock state.

36. The method of claim 35, further comprising:

disregarding the edges detected during periods other than the first and second periods.

37. The method of claim 35, further comprising:

generating the bit clock based on one of the channel bit interval and the first count value while maintaining the bit clock lock ready state if neither the first edge count value nor the second edge count value is equal to the first predetermined value.

38. The method of claim 35, wherein the first period is set by using a first window signal generated based on the first count value, where the first count value is reset and created by counting the system clock when the first edge is detected.

39. The method of claim 38, wherein the second period is set by using a second window signal generated based on a second count value, where the second count value is reset and generated by counting the system clock when the first edge is detected during the first period, and the second count value is reset and created by counting the system clock every time one of the edges is detected during the second period.

40. The method of claim 35, wherein generating the bit clock is performed while giving priority to the first count value over the channel bit interval.